Cont A9

layer formed over a portion of said film, and a metal, metal silicide, or metal nitride film overlaying said film and said oxide layer.

REMARKS

Claims 17-20, 29 and 30 were restricted and are now cancelled. Claims 1-16 and 21-28 have been amended. New claims 31-40 are added to protect various embodiments of the invention not previously claimed. Support for the newly entered claims is provided for in the specification and drawing figures; no new matter has been entered. Therefore, claims 1-16, 21-28, and 31-40 are pending in this application.

35 U.S.C. § 112

Claims 1-16 and 21-28 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for the reasons noted in the official action. The rejected claims are accordingly amended, by the above claim amendments, and the presently pending claims are now believed to particularly point out and distinctly claim the subject matter regarded as the invention, thereby overcoming all of the raised § 112, second paragraph, rejections.

35 U.S.C. § 103

Claims 1-3, 6-11, 13-16 and 21-26 are rejected under 35 USC 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in combination with Kizilyalli et al (US 6,174,807). Kizilyalli et al disclose a multi-layered dual-doped polysilicon structure that minimizes Boron penetration into the n+ polysilicon during formation of the p+ polysilicon. In particular, Kizilyalli et al disclose forming n+ polysilicon in the polysilicon layer above the p-tub region of the substrate, and then forming a p+ gate dopant barrier in the n+ polysilicon. Kizilyalli et al disclose that although the p+ gate dopant barrier 50 is depicted as a separate and discrete layer, the p+ gate dopant barrier 50 is preferably comprised of nitrogen implanted into and concentrated near the surface of the polysilicon layer 20 above the p-tub region 24. See FIG. 3 and column 3, lines 5-10. Kizilyalli et al also suggest that an argon-rich region may also be a suitable barrier. Id., line 1. Accordingly, Kizilyalli et al combined with the AAPA fail to teach or suggest

the limitation of an oxide diffusion barrier layer formed in the polysilicide gate electrode structure, as recited by amended independent claims 1-3, 6-11, and 13-16. As amended claims 21-26 also depend from unobvious claim 1, Applicants assert that these claims are also unobvious in view of the cited art.

Claims 4, 5, and 27 are rejected as being unpatentable over AAPA in combination with Kizilyalli et al as applied to claims 1-3, 6-11, 13-16 and 21-26, and further in view of Fuji et al (US 5,355,010). As pointed out above, Kizilyalli et al discloses a nitrogen or argon-rich diffuse barrier layer implanted into and concentrated near the surface of the polysilicon layer above the p-tub region of semiconductive structure. Fuji et al is cited for disclosing a CMOS structure, and therefore does not correct the above noted deficiency of Kizilyalli et al. Accordingly, the AAPA in combination with the Kizilyalli et al and further in view of Fuji et al, fail to teach or suggest the limitation of an oxide diffusion barrier layer formed in the polysilicide gate electrode structure, as recited by amended claims 4, 7, and 8 (from which claim 27 depends).

Claims 1-3, 6, 9-16 and 21-26 are rejected as being unpatentable over AAPA in combination with Hunter et al (US 5,940,725). Hunter et al disclose a silicon-rich nitride diffusion barrier layer 48, which is formed specifically by sputtering. See FIG. 2C and column 4, lines 12-18. Accordingly, the AAPA in combination with Hunter et al fail to teach or suggest the limitations of an oxide diffusion barrier layer formed in the polysilicide gate electrode structure, as recited by amended claims 1-3, 6, 9-16, and 21-26.

New Claims

With regards to new claims 31-40, none of the cited prior art reference teach or suggest the limitations of a gate electrode structure having an oxide layer formed over a portion of a film, and a metal, metal silicide, or metal nitride film overlaying the film and the oxide diffusion barrier layer.

Remaining Prior Art

The Applicants note the remaining prior art cited in the Official Action. As none of that additional art is applied by the Examiner against the claims of this application, the Applicants are not providing any comments concerning the same at this time.

CONCLUSION

Applicants respectfully submit that, in view of the above amendments and remarks the application is now in condition for allowance. The Examiner is encouraged to contact the undersigned to resolve efficiently any formal matters or to discuss any aspects of the application or of this response. Otherwise, early notification of allowable subject matter is respectfully solicited.

Respectfully submitted,

KILLWORTH, GOTTMAN, HAGAN &
SCHAEFF, L.L.P.

By _____
William A. Jividen
Registration No. 42,695

One Dayton Centre
One South Main Street, Suite 500
Dayton, Ohio 45402-2023
Telephone: (937) 223-2050
Facsimile: (937) 223-0724
e-mail: jividenw@kghs.com

Appendix

In the specification:

Please replace the paragraph on page 1, starting at line 7, with:

--Integrated circuit devices commonly employ a laminar or ~~polycilicide~~polysilicide structure composed of a polycrystalline silicon film and an overlying film of a metal, metal silicide, or metal nitride. In many cases, the polycrystalline silicon film comprises an N+ polysilicon region doped with an N type impurity and a P+ polysilicon region doped with a P type impurity. The present inventors have recognized that many P+ and N+ dopant materials are subject to migration from a given polysilicon layer to another polysilicon layer, to an overlying conductive layer, or to another region of the given polysilicon layer. As a result, these opposite types of impurities are subject to cross diffusion. This cross diffusion can lead to performance degradation in the integrated circuit device.--

Please replace the following paragraphs starting after the "BRIEF SUMMARY OF THE INVENTION" and ending on page 6, line 24, with:

--This need is met by the present invention wherein an ultrathin buried diffusion barrier layer (UBDBL) is formed over all or part of the doped polysilicon layer of a ~~polycilicide~~polysilicide structure composed of the polycrystalline silicon film and an overlying film of a metal, metal silicide, or metal nitride.

In accordance with one embodiment of the present invention, a memory cell is provided comprising a semiconductor substrate, a P well, an N well, an N type active region, a P type active region, an isolation region, a ~~polycilicide~~polysilicide gate electrode structure, and a diffusion barrier layer. The P well is formed in the semiconductor substrate. The N well is formed in the semiconductor substrate adjacent to the P well. The N type active region is defined in the P well and the P type active region is defined in the N well. The isolation region is arranged to isolate the N type active region from the P type active region. The ~~polycilicide~~polysilicide gate electrode

structure is composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film. The polycrystalline silicon film comprises an N+ polysilicon layer over the N type active region and a P+ polysilicon layer over the P type active region. The diffusion barrier layer is formed in the ~~polycilicide~~polysilicide gate electrode structure over a substantial portion of the polycrystalline silicon film between the polycrystalline silicon film and the metal, metal silicide, or metal nitride film.

In accordance with another embodiment of the present invention, a memory cell is provide comprising a semiconductor substrate, a P well, an N well, an NMOS transistor, a PMOS transistor, an isolation region, a ~~polycilicide~~polysilicide gate electrode structure, and a diffusion barrier layer. The P well is formed in the semiconductor substrate. The N well is formed in the semiconductor substrate. The NMOS transistor defines an N type active region in the P well. The PMOS transistor defining a P type active region in the N well. The isolation region is arranged to isolate the N type active region from the P type active region. The ~~polycilicide~~polysilicide gate electrode structure is composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film. The polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of the NMOS transistor and a P+ polysilicon layer forming a portion of the PMOS transistor. The diffusion barrier layer is formed in the ~~polycilicide~~polysilicide gate electrode structure over a substantial portion of the polycrystalline silicon film between the polycrystalline silicon film and the metal, metal silicide, or metal nitride film.

Preferably, the diffusion barrier layer comprises an ultrathin diffusion barrier layer and has a thickness of between about 5 Å and about 25 Å.

In accordance with yet another embodiment of the present invention, an SRAM memory cell is provided comprising a semiconductor substrate, a P well, an N well, a flip flop, an isolation region, a ~~polycilicide~~polysilicide gate electrode structure, and a diffusion barrier layer. The P well formed in the semiconductor substrate. The N well formed is in the semiconductor substrate. The flip-flop is formed by two access transistors and a pair of cross coupled inverters. Each pair of cross-coupled inverters includes a pull up transistor and a pull down transistor. The pull-up transistor defines a P type active region in the N well and the pull-down transistor defines an N type active

region in the P well. The isolation region is arranged to isolate the N type active region from the P type active region. The ~~polycilicide~~polysilicide gate electrode structure is composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film. The polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of the pull-down transistor and a P+ polysilicon layer forming a portion of the pull-up transistor. The diffusion barrier layer is formed in the ~~polycilicide~~polysilicide gate electrode structure between the polycrystalline silicon film and the metal, metal silicide, or metal nitride film over a substantial portion of the polycrystalline silicon film.

In accordance with yet another embodiment of the present invention, an SRAM memory cell is provided comprising a semiconductor substrate, a P well, an N well, a flip flop, an isolation region, a ~~polycilicide~~polysilicide gate electrode structure, and a diffusion barrier layer. The flip-flop is formed by two access transistors and a pair of cross coupled inverters. Each pair of cross-coupled inverters includes a pull up transistor and a pull down transistor. The pull-up transistor defines a P type active region in the N well and the pull-down transistor defines an N type active region in the P well. The isolation region is arranged to isolate the N type active region from the P type active region. The ~~polycilicide~~polysilicide gate electrode structure is composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film. The polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of the pull-down transistor and a P+ polysilicon layer forming a portion of the pull-up transistor. The diffusion barrier layer is formed in the ~~polycilicide~~polysilicide gate electrode structure between the polycrystalline silicon film and the metal, metal silicide, or metal nitride film over a substantial portion of the N+ polysilicon layer and the P+ polysilicon layer.

In accordance with yet another embodiment of the present invention, a memory cell array is provided comprising a plurality of SRAM cells arranged in rows and columns. Each cell of the array is connected to a word line and to a pair of bit lines and comprises a semiconductor substrate, a P well, an N well, a flip flop, an isolation region, a ~~polycilicide~~polysilicide gate electrode structure, and a diffusion barrier layer. The flip-flop is formed by two access transistors and a pair of cross coupled inverters. Each pair

of cross-coupled inverters includes a pull up transistor and a pull down transistor. The pull-up transistor defines a P type active region in the N well and the pull-down transistor defines an N type active region in the P well. The isolation region is arranged to isolate the N type active region from the P type active region. The ~~polycilicide~~polysilicide gate electrode structure is composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film. The polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of the pull-down transistor and a P+ polysilicon layer forming a portion of the pull-up transistor. The diffusion barrier layer is formed in the ~~polycilicide~~polysilicide gate electrode structure between the polycrystalline silicon film and the metal, metal silicide, or metal nitride film over a substantial portion of the polycrystalline silicon film.

In accordance with yet another embodiment of the present invention, a computer system is provided including a microprocessor in communication with a memory cell array via a data communication path. The memory cell array comprises a plurality of SRAM cells arranged in rows and columns. Each cell of the array is connected to a word line and to a pair of bit lines and comprises a semiconductor substrate, a P well, an N well, a flip flop, an isolation region, a ~~polycilicide~~polysilicide gate electrode structure, and a diffusion barrier layer. The flip-flop is formed by two access transistors and a pair of cross coupled inverters. Each pair of cross-coupled inverters includes a pull up transistor and a pull down transistor. The pull-up transistor defines a P type active region in the N well and the pull-down transistor defines an N type active region in the P well. An isolation region is arranged to isolate the N type active region from the P type active region. A ~~polycilicide~~polysilicide gate electrode structure is composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film. The polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of the pull-down transistor and a P+ polysilicon layer forming a portion of the pull-up transistor. The diffusion barrier layer is formed in the ~~polycilicide~~polysilicide gate electrode structure between the polycrystalline silicon film and the metal, metal silicide, or metal nitride film over a substantial portion of the polycrystalline silicon film.

In accordance with yet another embodiment of the present invention, a method of fabricating an SRAM memory cell is provided. Recited in terms of physical location, as opposed to chronological order of processing, the method comprises the steps of (i) providing a semiconductor substrate, (ii) forming a P well in the semiconductor substrate, (iii) forming an N well in the semiconductor substrate, (iv) forming a P type active region of a pull-up transistor in the N well, (v) forming a gate oxide layer and a conductive gate of the pull-up transistor over the P type active region, (vi) forming an N type active region of a pull-down transistor in the P well; (vii) forming a gate oxide layer and a conductive gate of the pull-down transistor over the N type active region, (viii) forming an isolation region between the N type active region and the P type active region, (ix) forming a polycrystalline silicon film over the pull-down transistor and the pull-up transistor, (x) doping selectively the polycrystalline silicon film to form an N+ polysilicon layer over the pull-down transistor and a P+ polysilicon layer over the pull-up transistor; (xi) forming a diffusion barrier layer over a substantial portion of the polycrystalline silicon film, and (xii) forming a metal, metal silicide, or metal nitride film over the doped polycrystalline silicon film and the diffusion barrier layer. The diffusion barrier layer is formed by selective chemical oxidation of the polycrystalline silicon film.

In accordance with yet another embodiment of the present invention, a method of fabricating a memory cell array by arranging a plurality of the SRAM cells in rows and columns and connecting each SRAM cell of the array to a word line and to a pair of bit lines is provided. Recited in terms of physical location, as opposed to chronological order of processing, each of the SRAM cells is fabricated by (i) providing a semiconductor substrate, (ii) forming a P well in the semiconductor substrate, (iii) forming an N well in the semiconductor substrate, (iv) providing a flip-flop including two access transistors and a pair of cross coupled inverters wherein each pair of cross-coupled inverters includes a pull up transistor and a pull down transistor and wherein the pull-up transistor defines a P type active region in the N well and the pull-down transistor defines an N type active region in the P well, (v) arranging an isolation region to isolate the N type active region from the P type active region, (vi) providing a ~~polycilicide~~polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying

metal, metal silicide, or metal nitride film, wherein the polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of the pull-down transistor and a P+ polysilicon layer forming a portion of the pull-up transistor, and (vii) forming a diffusion barrier layer in the ~~polycilicide~~polysilicide gate electrode structure between the polycrystalline silicon film and the metal, metal silicide, or metal nitride film over a substantial portion of the polycrystalline silicon film.

In accordance with yet another embodiment of the present invention, a method of fabricating a computer system is provided. The computer system is fabricated by arranging a microprocessor in communication with a memory cell array via a data communication path and fabricating the memory cell array by arranging a plurality of the SRAM cells in rows and columns and connecting each SRAM cell of the array to a word line and to a pair of bit lines. Recited in terms of physical location, as opposed to chronological order of processing, each of the SRAM cells is fabricated by (i) providing a semiconductor substrate, (ii) forming a P well in the semiconductor substrate, (iii) forming an N well in the semiconductor substrate, (iv) providing a flip-flop including two access transistors and a pair of cross coupled inverters, wherein each pair of cross-coupled inverters includes a pull up transistor and a pull down transistor, and wherein the pull-up transistor defines a P type active region in the N well and the pull-down transistor defines an N type active region in the P well, (v) arranging an isolation region to isolate the N type active region from the P type active region, (vi) providing a ~~polycilicide~~polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein the polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of the pull-down transistor and a P+ polysilicon layer forming a portion of the pull-up transistor, (vii) forming a diffusion barrier layer in the ~~polycilicide~~polysilicide gate electrode structure between the polycrystalline silicon film and the metal, metal silicide, or metal nitride film over a substantial portion of the polycrystalline silicon film.--

Please replace the first paragraph on page 9, with

--The gate electrode structure of the CMOS structure **4** is constructed to have a laminar or ~~polycilicide~~polysilicide structure composed of a polycrystalline silicon film and an overlying film of a metal, metal silicide, or metal nitride. Specifically, the polycrystalline silicon film comprises an N+ polysilicon layer **21** formed over the NMOS transistor **11** and a P+ polysilicon layer **22** formed over the PMOS transistor **12**. Each of the polysilicon layers **21**, **22** typically provide a connection to a transistor gate. The N+ polysilicon layer **21** is doped with an N type impurity such as arsenic (As) or phosphorous P31. The P+ polysilicon layer **22** is doped with an N type impurity such as boron (B). The overlying metal, metal silicide, or metal nitride layer **24** is typically formed of a tungsten silicide (WSi_X: x=**2**, for example) and contributes to an accelerated signal transmission rate because the specific resistance of the metal, metal silicide, or metal nitride layer **24** is lower than that of the polycrystalline silicon layers **21**, **22**. The metal, metal silicide, or metal nitride layer **24** may be made of not only WSi_X but also molybdenum silicide $MoSi_X$, titanium silicide $TiSi_X$, tantalum silicide $TaSi_X$, cobalt silicide, nitrides of these metals, etc. An insulating capping layer **26** is formed over the WSi_X layer **24** and is typically formed of silicon dioxide or silicon nitride.--

Please replace the third paragraph on page 11, starting at line 15, with:

--In the embodiment illustrated in Fig. 5, the UBDBL **28** and the ~~polycilicide~~polysilicide gate electrode structure are arranged such that the UBDBL **28** is formed over a substantial portion of the P+ polysilicon layer **22** between the P+ polysilicon layer **22** and the metal, metal silicide, or metal nitride film **24** and does not extend over a substantial portion of the N+ polysilicon layer **21**. Stated differently, the UBDBL **28** is arranged such that the metal, metal silicide, or metal nitride film **24** is in direct contact with the N+ polysilicon layer **21** and defines an N type common boundary with the N+ polysilicon layer **21** that is significantly larger than any P type common boundary defined by the metal, metal silicide, or metal nitride film **24** and the P+

polysilicon layer **22**. The UBDBL **28** may be formed over the entire extent of that portion of the P+ polysilicon layer **22** that is overcoated by the metal, metal silicide, or metal nitride film **24**. In this manner, migration of P+ dopants from the P+ polysilicon layer **22** to the overlying metal, metal silicide, or metal nitride film **24** is significantly impeded by the UBDBL **28**. Although dopants from the N+ polysilicon layer **21** enter the overlying metal, metal silicide, or metal nitride film **24**, cross diffusion and P+ poly gate depletion are suppressed because these dopants, present in the overlying metal, metal silicide, or metal nitride film **24**, cannot cross the UBDBL **28** and enter the P+ polysilicon layer **22**.--

Please replace the paragraphs on page 12, starting at line 9, with:

--Similarly, in the embodiment illustrated in Fig. 6, the UBDBL **28** and the ~~polycilicide~~polysilicide gate electrode structure are arranged such that the UBDBL **28** is formed over a substantial portion of the N+ polysilicon layer **21** between the N+ polysilicon layer **21** and the metal, metal silicide, or metal nitride film **24** and does not extend over a substantial portion of the P+ polysilicon layer **22**. Stated differently, the UBDBL **28** is arranged such that the metal, metal silicide, or metal nitride film **24** is in direct contact with the P+ polysilicon layer **22** and defines an P type common boundary with the P+ polysilicon layer **22** that is significantly larger than any N type common boundary defined by the metal, metal silicide, or metal nitride film **24** and the N+ polysilicon layer **21**. The UBDBL **28** may be formed over the entire extent of that portion of the N+ polysilicon layer **21** that is overcoated by the metal, metal silicide, or metal nitride film **24**. In this manner, migration of N+ dopants from the N+ polysilicon layer **21** to the overlying metal, metal silicide, or metal nitride film **26** is significantly impeded by the UBDBL **28**. Although dopants from the P+ polysilicon layer **22** enter the overlying metal, metal silicide, or metal nitride film **24**, cross diffusion and N+ poly gate depletion are suppressed because these dopants, present in the overlying metal, metal silicide, or metal nitride film **24**, cannot cross the UBDBL **28** and enter the N+ polysilicon layer **21**.

Finally, in the embodiment illustrated in Fig. 7, the UBDBL **28** is formed in the ~~polycilicide~~polysilicide gate electrode structure over the N+ polysilicon layer **21** and the P+ polysilicon layer **22**. In this manner, migration of P+ dopants from the P+ polysilicon layer **22** and migration of N+ dopants from the N+ polysilicon layer **21** to the overlying metal, metal silicide, or metal nitride film **24** is significantly impeded by the UBDBL **28**. Cross diffusion and gate depletion are suppressed because the dopants cannot cross the UBDBL **28** and enter the opposite polysilicon layer.--

Please replace the ABSTRACT OF THE DISCLOSURE, with:

--According to the present invention, an ultrathin buried diffusion barrier layer (UBDBL) is formed over all or part of the doped polysilicon layer of a ~~polycilicide~~polysilicide structure composed of the polycrystalline silicon film and an overlying film of a metal, metal silicide, or metal nitride. More specifically, according to one embodiment of the present invention, a memory cell is provided comprising a semiconductor substrate, a P well, an N well, an N type active region, a P type active region, an isolation region, a ~~polycilicide~~polysilicide gate electrode structure, and a diffusion barrier layer. The P well is formed in the semiconductor substrate. The N well is formed in the semiconductor substrate adjacent to the P well. The N type active region is defined in the P well and the P type active region is defined in the N well. The isolation region is arranged to isolate the N type active region from the P type active region. The ~~polycilicide~~polysilicide gate electrode structure is composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film. The polycrystalline silicon film comprises an N+ polysilicon layer formed with the N type active region and a P+ polysilicon layer formed with the P type active region. The diffusion barrier layer is formed in the ~~polycilicide~~polysilicide gate electrode structure over a substantial portion of the polycrystalline silicon film between the polycrystalline silicon film and the metal, metal silicide, or metal nitride film.--

In the claims:

1. (Amended) A memory cell comprising:

a semiconductor substrate;

a P well formed in said semiconductor substrate;

an N well formed in said semiconductor substrate adjacent to said P well;

an N type active region defined in said P well;

a P type active region defined in said N well;

an isolation region arranged to isolate said N type active region from said P type active region;

a ~~polycilicide~~polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer over said N type active region and a P+ polysilicon layer over said P type active region; and

an oxide diffusion barrier layer formed in said ~~polycilicide~~polysilicide gate electrode structure over a ~~substantial~~ portion of said polycrystalline silicon film between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film.

2. (Amended) A memory cell comprising:

a semiconductor substrate;

a P well formed in said semiconductor substrate;

an N well formed in said semiconductor substrate;

an NMOS transistor defining an N type active region in said P well;

a PMOS transistor defining a P type active region in said N well;

an isolation region arranged to isolate said N type active region from said P type active region;

a ~~polycilicide~~polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said NMOS transistor and a P+ polysilicon layer forming a portion of said PMOS transistor; and

an oxide diffusion barrier layer formed in said ~~polycilicide~~polysilicide gate electrode structure over a ~~substantial~~ portion of said polycrystalline silicon film between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film.

3. (Amended) A memory cell comprising:

a semiconductor substrate;

a P well formed in said semiconductor substrate;

an N well formed in said semiconductor substrate;

an NMOS transistor defining an N type active region in said P well;

a PMOS transistor defining a P type active region in said N well;

an isolation region arranged to isolate said N type active region from said P type active region;

a ~~polycilicide~~polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said NMOS transistor and a P+ polysilicon layer forming a portion of said PMOS transistor; and

an oxide diffusion barrier layer formed in said ~~polycilicide~~polysilicide gate electrode structure between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film, wherein said ~~polycilicide~~polysilicide gate electrode structure and said oxide diffusion barrier layer are arranged such that migration of P+ dopants from said P+ polysilicon layer to said overlying metal, metal silicide, or metal nitride film is significantly impeded by said oxide diffusion barrier layer.

4. (Amended) A memory cell comprising:

a semiconductor substrate;

a P well formed in said semiconductor substrate;

an N well formed in said semiconductor substrate;

an NMOS transistor defining an N type active region in said P well;

a PMOS transistor defining a P type active region in said N well;

an isolation region arranged to isolate said N type active region from said P type active region;

a ~~polycilicide~~polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said NMOS transistor and a P+ polysilicon layer forming a portion of said PMOS transistor; and

an oxide diffusion barrier layer formed in said ~~polycilicide~~polysilicide gate electrode structure over a ~~substantial~~ portion of said P+ polysilicon layer between said P+ polysilicon layer and said metal, metal silicide, or metal nitride film, wherein said oxide diffusion barrier layer does not extend over a ~~substantial~~ portion of said N+ polysilicon layer.

5. (Amended) A memory cell comprising:

a semiconductor substrate;

a P well formed in said semiconductor substrate;

an N well formed in said semiconductor substrate;

an NMOS transistor defining an N type active region in said P well;

a PMOS transistor defining a P type active region in said N well;

an isolation region arranged to isolate said N type active region from said P type active region;

a ~~polycilicide~~polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said NMOS transistor and a P+ polysilicon layer forming a portion of said PMOS transistor; and

an oxide diffusion barrier layer formed in said ~~polycilicide~~polysilicide gate electrode structure over ~~a substantial portion of~~ said P+ polysilicon layer between said P+ polysilicon layer and said metal, metal silicide, or metal nitride film, wherein said oxide diffusion barrier layer is arranged such that said metal, metal silicide, or metal nitride

film defines an N type common boundary with said N+ polysilicon layer that is significantly larger than a P type common boundary defined by said metal, metal silicide, or metal nitride film and said P+ polysilicon layer.

6. (Amended) A memory cell comprising:

a semiconductor substrate;

a P well formed in said semiconductor substrate;

an N well formed in said semiconductor substrate;

an NMOS transistor defining an N type active region in said P well;

a PMOS transistor defining a P type active region in said N well;

an isolation region arranged to isolate said N type active region from said P type active region;

a ~~polycilicide~~polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said NMOS transistor and a P+ polysilicon layer forming a portion of said PMOS transistor; and

an oxide diffusion barrier layer formed in said ~~polycilicide~~polysilicide gate electrode structure between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film, wherein said ~~polycilicide~~polysilicide gate electrode structure and said oxide diffusion barrier layer are arranged such that migration of N+ dopants from said N+ polysilicon layer to said overlying metal, metal silicide, or metal nitride film is significantly impeded by said oxide diffusion barrier layer.

7. (Amended) A memory cell comprising:

a semiconductor substrate;

a P well formed in said semiconductor substrate;

an N well formed in said semiconductor substrate;

an NMOS transistor defining an N type active region in said P well;

a PMOS transistor defining a P type active region in said N well;

an isolation region arranged to isolate said N type active region from said P type active region;

a ~~polycilicide~~polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said NMOS transistor and a P+ polysilicon layer forming a portion of said PMOS transistor; and

an oxide diffusion barrier layer formed in said ~~polycilicide~~polysilicide gate electrode structure over a ~~substantial~~ portion of said N+ polysilicon layer between said N+ polysilicon layer and said metal, metal silicide, or metal nitride film, wherein said oxide diffusion barrier layer does not extend over a ~~substantial~~ portion of said P+ polysilicon layer.

8. (Amended) A memory cell comprising:

a semiconductor substrate;

a P well formed in said semiconductor substrate;

an N well formed in said semiconductor substrate;

an NMOS transistor defining an N type active region in said P well;

a PMOS transistor defining a P type active region in said N well;

an isolation region arranged to isolate said N type active region from said P type active region;

a ~~polycilicide~~polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said NMOS transistor and a P+ polysilicon layer forming a portion of said PMOS transistor; and

an oxide diffusion barrier layer formed in said ~~polycilicide~~polysilicide gate electrode structure over a ~~substantial~~ portion of said N+ polysilicon layer between said N+ polysilicon layer and said metal, metal silicide, or metal nitride film, wherein said oxide diffusion barrier layer is arranged such that said metal, metal silicide, or metal

nitride film defines a P type common boundary with said P+ polysilicon layer that is significantly larger than an N type common boundary defined by said metal, metal silicide, or metal nitride film and said N+ polysilicon layer.

9. (Amended) A memory cell comprising:

a semiconductor substrate;

a P well formed in said semiconductor substrate;

an N well formed in said semiconductor substrate;

an NMOS transistor defining an N type active region in said P well;

a PMOS transistor defining a P type active region in said N well;

an isolation region arranged to isolate said N type active region from said P type active region;

a ~~polycilicide~~polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said NMOS transistor and a P+ polysilicon layer forming a portion of said PMOS transistor; and

an oxide diffusion barrier layer formed in said ~~polycilicide~~polysilicide gate electrode structure over said N+ polysilicon layer and said P+ polysilicon layer between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film, wherein said ~~polycilicide~~polysilicide gate electrode structure and said oxide diffusion barrier layer are arranged such that

migration of P+ dopants from said P+ polysilicon layer to said overlying metal, metal silicide, or metal nitride film is significantly impeded by said oxide diffusion barrier layer and

migration of N+ dopants from said N+ polysilicon layer to said overlying metal, metal silicide, or metal nitride film is significantly impeded by said oxide diffusion barrier layer.

10. (Amended) An SRAM memory cell comprising:

a semiconductor substrate;

a P well formed in said semiconductor substrate;

an N well formed in said semiconductor substrate;

a flip-flop formed by two access transistors and a pair of cross coupled inverters, wherein each pair of cross-coupled inverters includes a pull up transistor and a pull down transistor, and wherein said pull-up transistor defines a P type active region in said N well and said pull-down transistor defines an N type active region in said P well;

an isolation region arranged to isolate said N type active region from said P type active region;

a ~~polycilicide~~polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said pull-down transistor and a P+ polysilicon layer forming a portion of said pull-up transistor; and

an oxide diffusion barrier layer formed in said ~~polycilicide~~polysilicide gate electrode structure between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film over a ~~substantial~~ portion of said polycrystalline silicon film.

11. (Amended) An SRAM memory cell comprising:

a semiconductor substrate;

a P well formed in said semiconductor substrate;

an N well formed in said semiconductor substrate;

a flip-flop formed by two access transistors and a pair of cross coupled inverters, wherein each pair of cross-coupled inverters includes a pull up transistor and a pull down transistor, and wherein said pull-up transistor defines a P type active region in said N well and said pull-down transistor defines an N type active region in said P well;

an isolation region arranged to isolate said N type active region from said P type active region;

a ~~polycilicide~~polysilicide gate electrode structure composed of a polycrystalline silicon film having a thickness of between about 500 Å and about 4000 Å and an overlying metal, metal silicide, or metal nitride film having a thickness of between about 500 Å and 4000 Å, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said pull-down transistor and a P+ polysilicon layer forming a portion of said pull-up transistor; and

an oxide diffusion barrier layer having a thickness of between about 3~~10~~ Å and about 25~~15~~ Å formed in said ~~polycilicide~~polysilicide gate electrode structure between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film over a ~~substantial~~ portion of said polycrystalline silicon film.

12. (Amended) An SRAM memory cell comprising:

a semiconductor substrate;

a P well formed in said semiconductor substrate;

an N well formed in said semiconductor substrate;

a flip-flop formed by two access transistors and a pair of cross coupled inverters, wherein each pair of cross-coupled inverters includes a pull up transistor and a pull down transistor, and wherein said pull-up transistor defines a P type active region in said N well and said pull-down transistor defines an N type active region in said P well;

an isolation region arranged to isolate said N type active region from said P type active region;

a ~~polycilicide~~polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said pull-down transistor and a P+ polysilicon layer forming a portion of said pull-up transistor; and

an oxide diffusion barrier layer formed in said ~~polycilicide~~polysilicide gate electrode structure between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film over a ~~substantial~~ portion of said N+ polysilicon layer and said P+ polysilicon layer.

13. (Amended) An SRAM memory cell comprising:

a semiconductor substrate;

a P well formed in said semiconductor substrate;

an N well formed in said semiconductor substrate;

a flip-flop formed by two access transistors and a pair of cross coupled inverters, wherein each pair of cross-coupled inverters includes a pull up transistor and a pull down transistor, and wherein said pull-up transistor defines a P type active region in said N well and said pull-down transistor defines an N type active region in said P well;

an isolation region arranged to isolate said N type active region from said P type active region;

a ~~polycilicide~~polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said pull-down transistor and a P+ polysilicon layer forming a portion of said pull-up transistor; and

an oxide diffusion barrier layer formed in said ~~polycilicide~~polysilicide gate electrode structure between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film, wherein said ~~polycilicide~~polysilicide gate electrode structure and said oxide diffusion barrier layer are arranged such that migration of P+ dopants from said P+ polysilicon layer to said overlying metal, metal silicide, or metal nitride film is significantly impeded by said oxide diffusion barrier layer.

14. (Amended) An SRAM memory cell comprising:

a semiconductor substrate;

a P well formed in said semiconductor substrate;

an N well formed in said semiconductor substrate;

a flip-flop formed by two access transistors and a pair of cross coupled inverters, wherein each pair of cross-coupled inverters includes a pull up transistor and a pull down

transistor, and wherein said pull-up transistor defines a P type active region in said N well and said pull-down transistor defines an N type active region in said P well;

an isolation region arranged to isolate said N type active region from said P type active region;

a ~~polycilicide~~polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said pull-down transistor and a P+ polysilicon layer forming a portion of said pull-up transistor; and

an oxide diffusion barrier layer formed in said ~~polycilicide~~polysilicide gate electrode structure between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film, wherein said ~~polycilicide~~polysilicide gate electrode structure and said oxide diffusion barrier layer are arranged such that migration of N+ dopants from said N+ polysilicon layer to said overlying metal, metal silicide, or metal nitride film is significantly impeded by said oxide diffusion barrier layer.

15. (Amended) A memory cell array comprising a plurality of SRAM cells arranged in rows and columns, wherein each cell of said array is connected to a word line and to a pair of bit lines and comprises:

a semiconductor substrate;

a P well formed in said semiconductor substrate;

an N well formed in said semiconductor substrate;

a flip-flop formed by two access transistors and a pair of cross coupled inverters, wherein each pair of cross-coupled inverters includes a pull up transistor and a pull down transistor, and wherein said pull-up transistor defines a P type active region in said N well and said pull-down transistor defines an N type active region in said P well;

an isolation region arranged to isolate said N type active region from said P type active region;

a ~~polycilicide~~polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said

polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said pull-down transistor and a P+ polysilicon layer forming a portion of said pull-up transistor; and

an oxide diffusion barrier layer formed in said ~~polycilicide~~polysilicide gate electrode structure between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film over a ~~substantial~~ portion of said polycrystalline silicon film.

16. (Amended) A computer system including a microprocessor in communication with a memory cell array via a data communication path, wherein said memory cell array comprises a plurality of SRAM cells arranged in rows and columns, and wherein each cell of said array is connected to a word line and to a pair of bit lines and comprises:

a semiconductor substrate;

a P well formed in said semiconductor substrate;

an N well formed in said semiconductor substrate;

a flip-flop formed by two access transistors and a pair of cross coupled inverters, wherein each pair of cross-coupled inverters includes a pull up transistor and a pull down transistor, and wherein said pull-up transistor defines a P type active region in said N well and said pull-down transistor defines an N type active region in said P well;

an isolation region arranged to isolate said N type active region from said P type active region;

a ~~polycilicide~~polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said pull-down transistor and a P+ polysilicon layer forming a portion of said pull-up transistor; and

an oxide diffusion barrier layer formed in said ~~polycilicide~~polysilicide gate electrode structure between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film over a ~~substantial~~ portion of said polycrystalline silicon film.

21. (Amended) A memory cell as claimed in claim ~~12~~ wherein said oxide diffusion barrier layer comprises silicon dioxide~~an ultrathin diffusion barrier layer~~.

22. (Amended) A memory cell as claimed in claim ~~21~~ wherein said oxide~~ultrathin~~ diffusion barrier layer has a thickness of less than 125 Å.

23. (Amended) A memory cell as claimed in claim ~~21~~ wherein said oxide~~ultrathin~~ diffusion barrier layer has a thickness of between about 10 Å and about 15 Å.

24. (Amended) A memory cell as claimed in claim ~~21~~ wherein said oxide~~ultrathin~~ diffusion barrier layer has a thickness of between about 3 Å and about 125 Å.

25. (Amended) A memory cell as claimed in claim ~~21~~ wherein said oxide~~ultrathin~~ diffusion barrier layer has a thickness of between about 3 Å and about 50 Å.

26. (Amended) A memory cell as claimed in claim ~~21~~ wherein said oxide~~ultrathin~~ diffusion barrier layer has a thickness of between about 3 Å and about 125 Å and said polycrystalline silicon film has a thickness of between about 500 Å and about 4000 Å.

27. (Amended) A memory cell as claimed in claim 5 wherein metal, metal silicide, or metal nitride film form defines an overcoated portion of said P+ polysilicon layer and wherein said oxide diffusion barrier layer is formed in said ~~polycilicide~~polysilicide gate electrode structure between said metal, metal silicide, or metal nitride film and said P+ polysilicon layer over the entire extent of said overcoated portion of said P+ polysilicon layer.

28. (Amended) A memory cell as claimed in claim 8 wherein metal, metal silicide, or metal nitride film form defines an overcoated portion of said N+ polysilicon layer and wherein said oxide diffusion barrier layer is formed in said ~~polycilicide~~polysilicide gate

electrode structure between said metal, metal silicide, or metal nitride film and said N+ polysilicon layer over the entire extent of said overcoated portion of said N+ polysilicon layer.